11-15 70

A

jc760 U.S. PTO 11/13/00

UTILITY PATENT APPLICATION TRANSMITTAL

Attorney Docket No. **ONX-109**	Total Pages
First Named Inventor **MICHAEL J. DANEMAN**	
Title **FABRICATION AND CONTROLLED RELEASE OF STRUCTURES USING ETCH-STOP TRENCHES**	

jc430 U.S. PTO 09/712420 11/13/00

APPLICATION ELEMENTS	ACCOMPANYING APPLICATION PARTS
1. [X] Fee Transmittal Form	8. [X] Assignment cover sheet and document(s)
2. [X] Specification Total Pages: [13]	9. [X] Power of Attorney by Assignee
3. [X] Drawing(s) Total Sheets: [3]	[ ] with CFR 3.73(b) statement
4. [X] Oath or Declaration Total Pages: [1]	10. [ ] English Translation Document
a. [X] Newly executed (original or copy)	11. [ ] IDS/PTO-1449
b. [ ] Copy from a prior application 1.63(d) (complete Box 17 and note Box 5 below)	[ ] with copies of cited references
i. [ ] Signed statement deleting inventors named in the prior application, see CFR 1.63(d)(2) and 1.33(b)	12. [ ] Preliminary Amendment
5. [ ] Incorporation by Reference (if 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated therein by reference.	13. [X] Return Receipt Postcard (MPEP 503)
6. [ ] Microfiche Computer Program *(Appendix)*	14. [x] Small Entity Statement
7. [ ] Nucleotide/Amino Acid Sequence Submission (all the following are necessary)	[ ] Statement filed in prior application Status still proper and desired
a. [ ] Computer Readable Copy	15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
b. [ ] Paper Copy (identical to computer copy)	16. [x] Other: **Preliminary Amendment A**
c. [ ] Statement verifying identity of above copies	

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

[ ] continuation [ ] divisional [ ] CIP ...of prior application No.: [ ]

18. CORRESPONDENCE ADDRESS

NAME	**JOSHUA D. ISENBERG LUMEN INTELLECTUAL PROPERTY SERVICES**				
ADDRESS	**45 CABOT AVENUE, SUITE 110**				
CITY	**SANTA CLARA**	STATE	**CA**	ZIP CODE	**95051**
COUNTRY	**USA**	TELEPHONE	**(408) 260-7300**	FAX	**(408) 260-7301**

Certificate of Mailing by "Express Mail"

I hereby certify that I am mailing this correspondence on the date indicated below to the ASSISTANT COMMISSIONER FOR PATENTS, BOX PATENT APPLICATION, WASHINGTON, DC 20231 using the "Express Mail Post Office to Addressee" service of the United States Postal Service under 37 CFR 1.10.

SIGNATURE

DATE OF MAILING: 11/13/00

EXPRESS MAIL LABEL NO: EF 396742827 US

JENNIFER ANN PATTERSON

NAME OF PERSON SIGNING

FEE TRANSMITTAL

Application Number:	**Not assigned**
Filing Date:	**Filed herewith**
First Named Inventor:	**Michael J. Daneman**
Title of Invention:	**Fabrication and Controlled Release of Structures Using Etch-Stop Trenches**
Group Art Unit:	**Not assigned**
Examiner:	**Not assigned**
Attorney Docket No.:	**ONX-109**

Fee Calculation:
for [ ] Large Entity / [X] Small Entity.

Basic Billing Fee:

[X] Utility Patent Application:	$710 / $355	$ **355**
[ ] Provisional Patent Application:	$150 / $75	$

Claims:

[X] Number of Total Claims Over 20: [2]	x $18 / $9 =	$ **18**
[ ] No. of Independent Claims Over 3: [1]	x $80 / $40 =	$ **40**

Other Fees:

[ ] Extension of time, 1 month	$110 / $55	$
[ ] Extension of time, 2 months	$390 / $195	$
[ ] Extension of time, 3 months	$890 / $445	$
[ ] Extension of time, 4 months	$1390 / $695	$
[ ] Missing Parts Surcharge (Regular Application)	$130 / $65	$
[ ] Missing Parts Surcharge (Provisional Application)	$50 / $25	$
[X] Recordation of Assignment Document	$40	$ **40**
[ ] Issue Fee	$1240 / $620	$
[ ] Printed Patent; Number of Copies: [ ]	x $3 =	$

TOTAL PAYMENT: $ **453**

Method of Payment:
[X] Payment Enclosed
[X] Check

Signature of Applicant, Attorney, or Agent

Joshua D. Isenberg — 11/9/2000

Joshua D. Isenberg, Reg. No. 41,088 — Date

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(d)) – SMALL BUSINESS CONCERN

Application No.: Not assigned
Filing Date: Filed herewith
Applicant(s): Michael J. Daneman et al.
Title: Fabrication and Controlled Release of Structures Using Etch-Stop Trenches

I hereby declare that I am the owner of, or an official empowered to act on behalf of, the entity identified below:

Name of Concern: Onix Microsystems, Inc.

Address of Concern: 4138 Lakeside Drive
Richmond, CA 94801

I hereby declare that the concern identified above qualifies as a small business concern as defined in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention identified above and described in the application for Letters Patent filed herewith.

If the rights held by the concern identified above are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name:	ONIX MICROSYSTEMS INC.	[ ] Individual
Address:		[X] Small Business Concern
		[ ] Nonprofit Organization

I acknowledge the duty to file, in this application for patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

ASSIGNEE: Onix Microsystems, Inc.
4138 Lakeside Drive
Richmond, CA 94801

Official Authorized to Act on Behalf of Assignee:

Signature: Jim Hood

Name: Jim Hood

Title: VP Engr.

11/7/00
Date

IN THE US PATENT AND TRADEMARK OFFICE

Application Number:	Not yet assigned
Agent's Docket Number	ONX-109
Filing Date:	Not yet assigned
Applicant:	M. Daneman et al.
Application Title:	Fabrication of and Controlled Release of Structures Using Etch-Stop Trenches
Examiner:	Not Yet Assigned
Art Unit:	Not Yet Assigned

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231, on 11/13/02 (date of deposit).

[signature]
Name of Person Signing JENNIFER ADDY PETURSSON

11/13/02
date

PRELIMINARY AMENDMENT A

Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

Kindly amend the above application as follows:

SPECIFICATION:

At page 2, line 30, please change "filled" to --lined or filled--;

at page 2, line 31, after "etch-stop material" add --to form etch-stop trenches--;

at page 2, line 33, change "filled trenches" to --etch-stop trenches--;

at pg. 3, line 28, please add --Figs. **4A-4F** depict cross-sectional schematic diagrams illustrating formation of a MEMS device according to an alternative embodiment of the present invention;--;

at page 4 lines 30-31, rewrite "The trenches **108** are then completely filled with an etch-stop material **110** as shown in Fig. **1C**." as --An etch stop material **110** is then deposited in selected trenches **108** to fill or line them as shown in Fig. **1C**.--;

at page 4, lines 31-32, rewrite "The etch-stop material completely fills the trenches, forming filled trenches **110**." as --The etch-stop material lines or fills selected trenches, forming etch-stop trenches **112**.--;

at page 5, line 30, at page 6 line 3, and at page 6 line 4 change all instances of "filled trenches **112**" to --etch-stop trenches **112**--;

at page 6, line 27, please change "completely filled" to --lined or filled--;

at page 6, line 29, please change "filled" to --etch-stop--;

at page 7, line 20, please change "filled trenches **212**" to --etch-stop trenches **212**--;

at page, 8, line 20, after "scope of the invention.", kindly add the following:

--For example, the structural features may be formed from portions of a device layer that are protected from etching by adjacent etch-stop layers. By way of example, Figs. **4A-4F** depict the fabrication of a MEMS structure using a starting material **401** having a substrate layer, two device layers and two etch stop layers. In Fig. **4A**, the process starts with a material **401** having upper and lower device layers **402**, **404**, disposed on a substrate **406**. A first etch-stop layer **403** is disposed between the upper and lower device layers **402**, **404**. A second etch-stop layer **403** is disposed between the lower device layer **404** and the substrate **406**. The device layers **402**, **404** may be layers of material such as silicon, glass, or quartz bonded or deposited on top of a substrate. The etch-stop layers **403** and **405** may include silicon oxide, silicon, or other applicable material. An example of material **401** would be a two-layer silicon-on-insulator (SOI) material. The material **401** may be patterned and etched to form one or more narrow trenches **408** in the device layers **402**, **404** and the first etch-stop layer **403** as shown in Fig. **4B**. The trenches **408** may optionally penetrate into the etch-stop layer **405** and/or the substrate **406**. The trenches **408** are then filled or lined with an etch-stop material to form one or more etch-stop trenches **411** as shown in Fig. **4C**. Selected portions of the upper device layer **402** are then etched to a stopping point, e.g., on the etch-stop layer **403** or device layer **404**. A layer of etch-stop material **413** is then deposited over the remaining portions of the upper device layer **402** and, optionally, also over lower device

layer **404** as shown in Fig. **4D**. Vias **414** are then etched in the first etch stop layer **403** as shown in Fig. **4E**. The vias **414** allow the etching of the lower device layer **404** to release a structure **415** formed by a portion of the upper device layer **402** that is bounded by the etch stop layers **403** and **413** as shown in Fig. **4F**. Specifically, the etch stop layers **403**, **413** may protect the structure **415** during an isotropic etch process that removes a portion of the lower device layer **404** bounded by the first and second etch stop layers **403**, **405** and the etch-stop trenches **411** to release the structure **415**.--.

DRAWINGS:

Kindly add Figs. **4A-4F** as shown in the attached drawing sheets.

CLAIMS:

Amend claims **1**, **17**, and **18** and add new claims as shown below:

1. (AMENDED) A method for a controlled release of structures comprising:

a) forming one or more trenches in a layer of device material;

b) **[filling the trenches with]** <u>depositing</u> an etch-stop material <u>in one or more selected trenches to form one or more etch-stop trenches</u>;

c) defining one or more structures between <u>the</u> selected **[filled]** trenches; and

d) etching one or more portions of the device layer between the **[filled]** <u>etch-stop</u> trenches to release the structures, wherein the etching does not etch the etch-stop material.

16. (AMENDED) A process for forming structures comprising:

i) forming one or more trenches in a layer of device material;

ii) **[filling the trenches with an]** <u>depositing an</u> etch-stop material <u>in selected trenches</u> to define one or more structures;

iii) masking a surface of the layer of device material to expose one or more selected areas of device material that border one or more **[filled]** <u>of the selected</u> trenches; and

iv) etching one or more of the selected areas of the device layer to release the structures, wherein the etching does not etch the etch-stop material.

17. (AMENDED) A comb structure comprising

a) one or more static comb fingers

b) one or more movable comb fingers that are movable with respect to the static comb fingers; wherein the static comb fingers, the movable comb fingers, or both are formed by:

i) forming one or more trenches in a layer of device material;

ii) **[filling the trenches with]** <u>depositing</u> an etch-stop material <u>in selected trenches</u> to define one or more structures

iii) masking a surface of the layer of device material to expose one or more selected areas of device

material that border one or more of the selected trenches; and

iv) etching one or more of the selected areas of the device layer to release the structures, wherein the etching does not etch the etch-stop material.

20. (AMENDED) A MEMS device, comprising one or more structures, wherein the structures have been formed by:

i) forming one or more trenches in a layer of device material;

ii) **[filling the trenches with]** depositing an etch-stop material in selected trenches to define one or more structures;

iii) masking a surface of the layer of device material to expose one or more selected areas of device material that border one or more **[filled]** of the selected trenches; and

iv) etching one or more of the selected areas of the device layer to release the structures, wherein the etching does not etch the etch-stop material.

23. (NEW) The method of claim 10, wherein the structural layer is protected by one or more etch-stop layers.

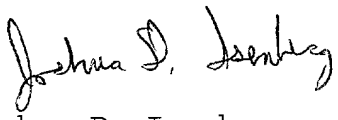
24. (NEW) The method of claim 16, wherein one or more of the structures include a device layer protected by one or more etch-stop layers.

25. (NEW) The device of claim 20, wherein one or more of the structures comprises a portion of a device layer bounded by one or more etch stop layers.

REMARKS:

The applicants submit that this preliminary amendment is being submitted concurrently with the filing of the present application. As such, no new matter is being entered with this amendment and entry of the amendment is proper.

Respectfully submitted,



Joshua D. Isenberg
Reg. No. 41,088
Patent Agent

Lumen
45 Cabot Ave.
Santa Clara, CA 95051
tel.: (408) 260-7300

Patent Application of

Michael J. Daneman, Berhang Behin

for

Fabrication and Controlled Release of Structures Using Etch-Stop Trenches

FIELD OF THE INVENTION

This invention relates generally to microelectromechanical systems (MEMS). More particularly, it relates to forming structures on MEMS devices.

CROSS REFERENCE TO RELATED APPLICATION

This application is based on Provisional application 60/192,144, filed March 24, 2000, which is herein incorporated by reference.

BACKGROUND

Large topology MEMS structures have applications for actuators, where the actuation force can be greatly increased by increasing the actuator area; optical devices, where high aspect ratios are needed to interact with optical beams, bio-MEMS, where high aspect ratio channels and sensors may be required; and a number of other applications where it is desirable to use a semiconductor compatible process to generate large topology structures.

A number of methods currently exist for forming large topology structures in MEMS processes, however, all have distinct disadvantages in process compatibility with following steps and/or in process complexity.

One common approach uses deep UV or X-ray lithography to define high aspect ratio features in photoresist or polymer and then electrodeposit metallic material inside the photoresist features. However, once the photoresist or polymer is removed, tall features are left on the wafer, preventing the use of standard resist and deposition processes for further processing. Also, the use of metallic materials to form the features prevents high temperature steps in further processing. Finally, this method requires the use of expensive X-ray lithography sources, which are not commonly used in semiconductor processing, for forming features.

Another method uses standard photoresist processing followed by a deep anisotropic etch (for example into the device layer of an SOI wafer) to form deep features. As in the previous method, this process leaves tall features on the wafer, preventing further standard processing. If the trenches formed by this process are narrow enough, they may be planarized by depositing a conformal film of sacrificial material, however, in this case the features are limited to having very small trenches (typically 2μm or less in depth) significantly limiting the types of structures that may be defined.

SUMMARY

The disadvantages associated with the prior art are overcome by the present invention of methods for fabrication and controlled release of structures. The structures may be fabricated on a substrate by forming one or more trenches in a device layer. The trenches are subsequently filled with an etch-stop material. Material in the device layer is then isotropically etched in selected portions bounded by one or more of the filled trenches. The etching undercuts one or more portions of the etch-stop material that has been deposited over the surface of the device layer. The etch-stop material

may be used to form structures that are released by the etch process. Alternatively, the structures may be formed by a different type of material deposited over the device layer and/or etch-stop material. This approach provides a controlled release method where the exact timing of the isotropic release etch becomes non-critical. Further, using this method, structures with significant topology may be fabricated while keeping the wafer topology to a minimum during processing until the very end of the process. The present invention also includes structures fabricated in accordance with the method outlined above. This embodiment of the invention is particularly suitable for comb drive structures, such as those used in MEMS devices.

DESCRIPTION OF THE FIGURES

Figs. **1A-1E** depict cross sectional schematic diagrams illustrating formation of a MEMS device according to a first embodiment of the invention;

Figs. **2A-2F** depict cross sectional schematic diagrams illustrating formation of a MEMS device according to a second embodiment of the invention;

Figs. **3A** depicts an isometric view of a comb structure manufactured according to a third embodiment of the invention;

Figs **3B-3C** depict cross sectional side views of alternative embodiments of comb structures manufactured according to the present invention.

DETAILED DESCRIPTION

Although the following detailed description contains many specifics for the purposes of illustration, anyone of ordinary skill in the art will appreciate that many variations and alterations to the following details are within the scope of the invention. Accordingly, the following preferred

embodiment of the invention is set forth without any loss of generality to, and without imposing limitations upon, the claimed invention.

A first exemplary embodiment of process is useful for forming high aspect ratio structures on a substrate and releasing structures formed on a substrate is shown in Figs. **1A-1E**. The structures are typically formed in a device layer **102**. The device layer **102** may be the top layer of a silicon-on-insulator (SOI) substrate, the substrate itself, or a glass, quartz, or oxide layer deposited on top of a substrate. In this embodiment, the structures are formed on and released from an SOI substrate **101** depicted in Fig. **1A**. The SOI substrate **101** generally comprises the device layer **102** disposed on an intermediate **104**, which is disposed on a substrate layer **106**. The device layer **102**, intermediate layer **104**, and substrate layer **106** may be made from semiconductor materials, e.g., Si, GaAs, etc., metals e.g., Al, Cu, Ti, W, Au, etc., or insulators, e.g. oxides. The device layer **102** and the substrate layer **106** may be made of the same material as each other. Generally, the intermediate layer **104** is made of a material that is different from that of the device and substrate layers. The material of the intermediate layer is preferably made from a material that is etchable by a process that does not attack the device layer **102** or the substrate layer **106**.

As shown in Fig. **1B**, narrow trenches **108** are formed in the device layer **102** by patterning a standard resist and etching the device layer. The trenches **108** are then completely filled with an etch-stop material **110** as shown in Fig. **1C**. Suitable etch-stop materials include silicon nitride, polycrystalline silicon, silicon dioxide, tungsten, etc. The etch-stop material is typically deposited using chemical vapor deposition. Alternatively, sputtering or electroplating may

be used to deposit the etch-stop material **110**. The etch-stop material completely fills the trenches, forming filled trenches **110**. The etch-stop material **110** may be also deposited over a surface of the device layer **102**, which would typically happen in the same deposition step. Alternatively, a separate deposition may be required for this. At this point the surface of the device layer **102** is largely planar and any further processing may be performed using standard semiconductor processes. Also, since the etch-stop material may be deposited at high temperature, further high-temperature processing is not prevented.

Once all processing has been performed, a photoresist and/or etch-stop material **110** is patterned to expose selected portions **114** of the device layer **102**, as shown in Fig. **1D**. The patterning of the etch-stop material **110** defines one or more structures **120** bounded by one or more of the filled trenches **110**. The etch-stop material **110** may be etched using standard semiconductor techniques, e.g., wet etch, plasma etch, etc. Although, the structures **120** are depicted as being entirely formed by the etch-stop material **110**, the structures **120** may include other materials in addition to the etch-stop material **110**. Next, an isotropic etch of device layer **102** is performed, as shown in Fig. **1E**. During this step the material in the exposed portions **114** of the device layer **102** is etched, but the etch-stop material is not etched. In the embodiment depicted in Figs. **1A-1E**, the insulator **104** is also resistant to the isotropic etch process. Thus, the isotropic etch removes material from portions of the device layer **102** that are bounded by one or more filled trenches **112** and the intermediate layer **104**. The isotropic etch may be a wet etch process or dry etch process or some combination of both. The isotropic etch undercuts and releases structures **120** defined on top of the device layer by the patterning depicted in Fig. **1D**. The structures **120** may be secured to the etch-stop

material **110** or the device layer **120** at some point or points outside the plane of the drawing in Fig. **1E**. The etch is contained by the etch-stop material **110** in the filled trenches **112**. Thus, the spacing of the filled trenches **112** controls the width of the undercut. At this point, the structures **120** are fully defined and the devices are ready for use or a final release, depending on the process.

In the process described above with respect to Figs. **1A-1E**, the structures **120** were formed from the etch-stop material. In an alternative embodiment, structures may be formed using a material different from the etch-stop material. An application of this process may be used, for example, to form comb structures for electrostatic actuators, capacitive sensors, or other applications. The process for fabricating such a structure is shown in Figs. **2A-2F**. In Fig. **2A**, the process starts with a substrate **201** having a device layer **202** disposed on an intermediate layer **204**, which is disposed on a substrate layer **206**. The device layer **202** may alternatively be the substrate itself, or a layer of device material such as glass, quartz, or oxide deposited on top of a substrate. The device layer **202** is patterned to define one or more features, e.g. using a standard resist. The features are then etched to form one or more narrow trenches **208** in the device layer **202**, as shown in Fig. **2A**. The trenches **208** may penetrate into the oxide layer **204** and/or the substrate layer **206**. The trenches **208** are then completely filled with an etch-stop material **210** as described with respect to Fig. **1C**, to form one or more filled trenches **212**. The etch-stop material may also be deposited on top of the device layer **202**.

Selected portions of the etch-stop material **210** are removed to expose selected portions of the device layer **202**, as shown in Fig. **2D**. Structural features **222**, such as comb fingers, are then formed on the exposed portions of the device layer **202**.

Alternatively, the structural features **222** may be formed directly on top of the etch-stop material **210** as opposed to the device layer **202**. The structural features **222** are typically made of a material that is different from the etch-stop material **210**. Alternatively, the features **222** may be formed from the same material, but in a later deposition step. The structural features **222** may be formed from a patterned structural layer containing multiple sub-layers of material. The structural features **222** are secured to the structural layer **202** at some point or points outside the plane of the drawing in Figs. **2E-2F**. Once all processing of the structural features **222** has been performed, the photoresist and/or the etch-stop layer is patterned to expose the device layer in appropriate places as shown in Fig. **2E**. Next, an isotropic etch of the device layer is performed as shown in Fig. **2F**. During this step the exposed device layer material will be etched, undercutting and releasing the structures on top of the device layer as described above with respect to Fig. **1E**. The etch is contained by the etch-stop material **210** in the filled trenches **212**, controlling the width of the undercut. At this point, the structures are fully defined and the devices are ready for use or a final release, depending on the process.

The above methods may be used to fabricate different types of structures. Such structures may have greater topology, i.e., greater heights above the device layer, than in the prior art. For example, Fig. **3A** depicts an embodiment of a comb structure manufactured according to the present invention. The comb structure **300** generally comprises a static comb member **301** having one or more comb fingers **302** and a movable comb member **303** having one or more comb fingers **304**. The fingers **302**, **304** of the fixed and movable comb members **301, 303** interdigitate. Such a structure is useful in a comb-drive actuator device. In one example of such an actuator, an electric field between

the fixed and movable comb fingers **302**, **304** causes the movable fingers **302** to deflect in response to an electrostatic force.

Although the fixed and movable comb fingers **302**, **304** are depicted as being at substantially the same level, other arrangements are possible. For example, in the side cross sectional view depicted in Fig. **3B** movable comb fingers **302'** are disposed above static comb fingers **304'**. In such a case a voltage between the static comb fingers **304'** and the movable comb fingers **302'** would produce an electric force that would cause the movable comb fingers **302'** to deflect downward. Alternatively, as depicted in the side cross sectional view in Fig. **3C** movable comb fingers **302"** are disposed below static comb fingers **304"**. In such a case a voltage between the static comb fingers **304"** and the movable comb fingers **302"** would produce an electric force that would cause the movable comb fingers **302"** to deflect upward.

It will be clear to one skilled in the art that the above embodiments may be altered in many ways without departing from the scope of the invention. Accordingly, the scope of the invention should be determined by the following claims and their legal equivalents.

CLAIMS

What is claimed is:

1. A method for a controlled release of structures comprising:
   a) forming one or more trenches in a layer of device material;
   b) filling the trenches with an etch-stop material;
   c) defining one or more structures between selected filled trenches; and
   d) etching one or more portions of the device layer between the filled trenches to release the structures, wherein the etching does not etch the etch-stop material.

2. The method of claim 1, wherein b) includes depositing etch-stop material over the surface of the device layer.

3. The method of claim 2 wherein c) includes forming one or more openings in the etch-stop material that has been deposited over the surface of the device layer.

4. The method of claim 2, wherein the etching undercuts one or more portions of the etch-stop material that has been deposited over the surface of the device layer.

5. The method of claim 1 where the layer of device material is disposed between two layers of etch-stop material.

6. The method of claim 1, wherein the device layer includes one or more layers of a silicon-on-insulator (SOI) substrate.

7. The method of claim 1, wherein the device layer is a layer of glass, quartz or oxide.

8. The method of claim 1, wherein d) includes a wet etch process.

9. The method of claim 1, wherein d) includes a dry etch process.

10. The method of claim 1, further comprising: forming a structural layer proximate one or more of the exposed areas of the device layer.

11. The method of claim 10, wherein the etch process in d) does not etch the structural layer.

12. The method of claim 10, further comprising releasing one or more portions of the structural layer.

13. The method of claim 10, wherein the etch process in d) releases one or more portions of the structural layer.

14. The method of claim 10, wherein the structural layer includes one or more structures that are formed directly on top of the etch-stop layer.

15. The method of claim 14, wherein the structural layer contains two or more sub-layers.

16. A process for forming structures comprising:

i) forming one or more trenches in a layer of device material;

ii) filling the trenches with an etch-stop material to define one or more structures;

iii) masking a surface of the layer of device material to expose one or more selected areas of device material that border one or more filled trenches; and

iv) etching one or more of the selected areas of the device layer to release the structures, wherein the etching does not etch the etch-stop material.

17. A comb structure comprising

a) one or more static comb fingers

b) one or more movable comb fingers that are movable with respect to the static comb fingers; wherein the static comb fingers, the movable comb fingers, or both are formed by:

i) forming one or more trenches in a layer of device material;

ii) filling the trenches with an etch-stop material to define one or more structures

iii) masking a surface of the layer of device material to expose one or more selected areas of device material that border one or more filled trenches; and

iv) etching one or more of the selected areas of the device layer to release the structures, wherein the etching does not etch the etch-stop material.

18. The comb structure of Claim 17 wherein both the static comb fingers and the movable comb fingers are formed on the same level.

19. The comb structure of Claim 17 wherein the movable comb fingers are disposed above the static comb fingers.

20. A MEMS device, comprising one or more structures, wherein the structures have been formed by:

i) forming one or more trenches in a layer of device material;

ii) filling the trenches with an etch-stop material to define one or more structures;

iii) masking a surface of the layer of device material to expose one or more selected areas of device material that border one or more filled trenches; and

iv) etching one or more of the selected areas of the device layer to release the structures, wherein the etching does not etch the etch-stop material.

21. The MEMS device of claim 20, wherein the structures comprise one or more comb fingers.

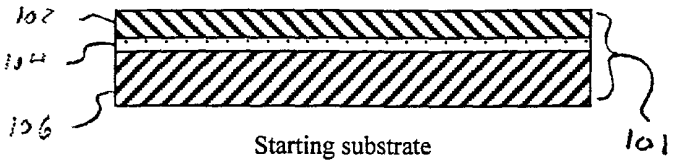
22. The MEMS device of claim 20, wherein the structures include one or more electrostatic actuators.

ONX-109

Fabrication and Controlled Release of Structures Using Etch-Stop Trenches

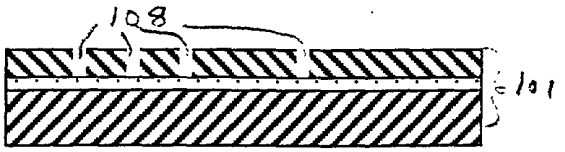
ABATRACT

MEMS structures may be formed on a substrate by forming a series trenches filled with etch-stop material in the device layer, followed by an isotropic etch of the device material stopping on the etch-stop material. This approach provides a controlled release method where the exact timing of the isotropic release etch becomes non-critical. Further, using this method, structures with significant topology may be fabricated while keeping the wafer topology to a minimum during processing until the very end of the process. Using the method of this invention, features with large topology may be formed while keeping the wafer topology to a minimum until the very end of the process.



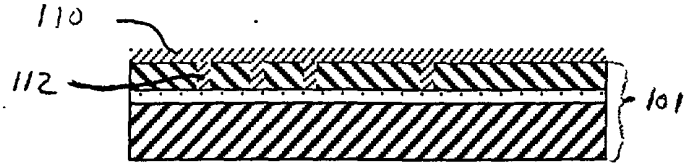
Starting substrate

Fig. 1A



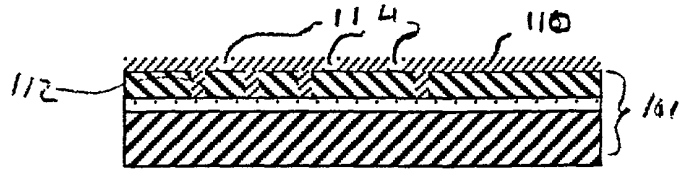
Trench formation

Fig. 1B



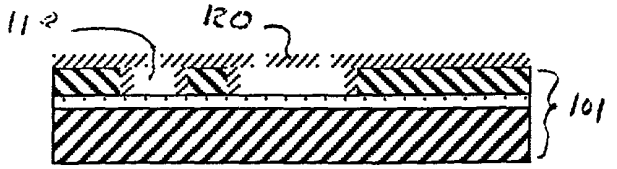
Trench fill with etch-stop material

Fig 1C



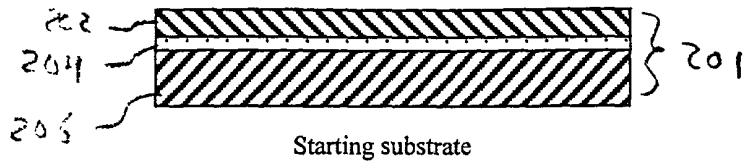
Selective masking of the device layer

Fig. 1D



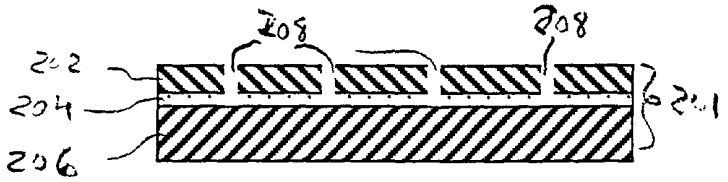
Isotropic release etch

Fig 1E



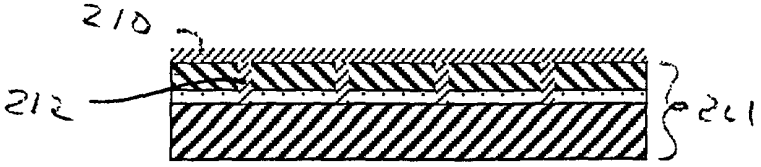
Starting substrate

Fig. 2A



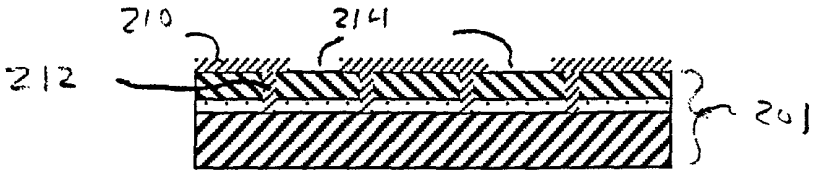
Trench formation

Fig. 2B



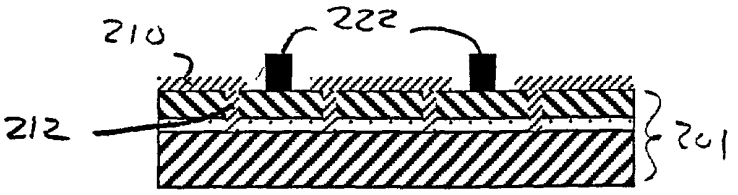
Trench fill with etch-stop material

Fig. 2C



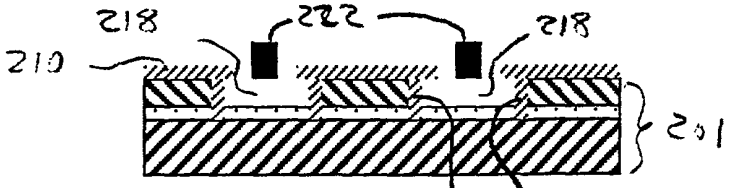
Selective exposure of device layer material

Fig. 2D



Formation of top comb fingers

Fig. 2E



Isotropic release etch

Fig. 2F

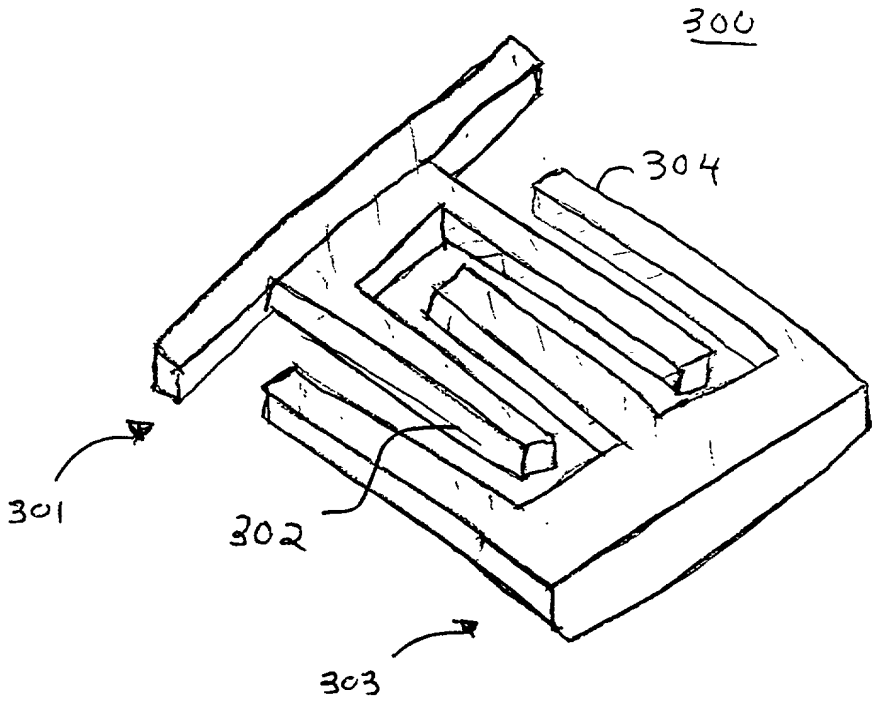


Fig. 3A

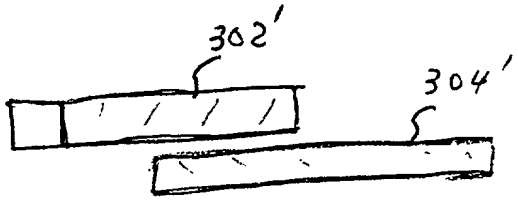


Fig. 3B

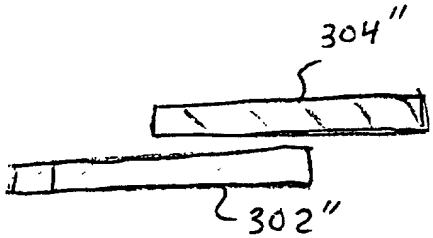


Fig. 3C

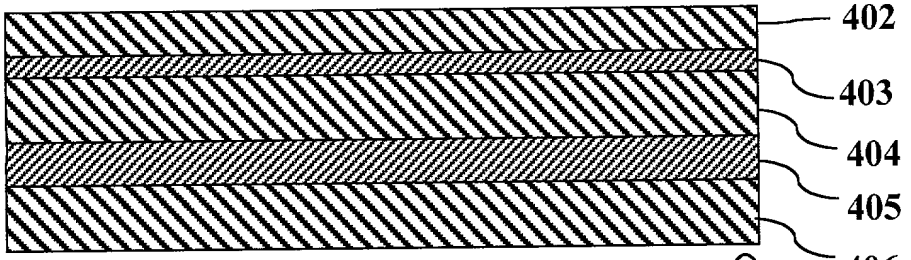


FIG 4A

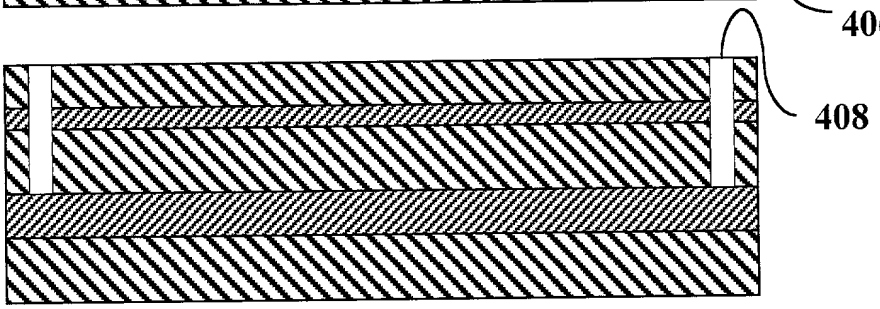


FIG 4B

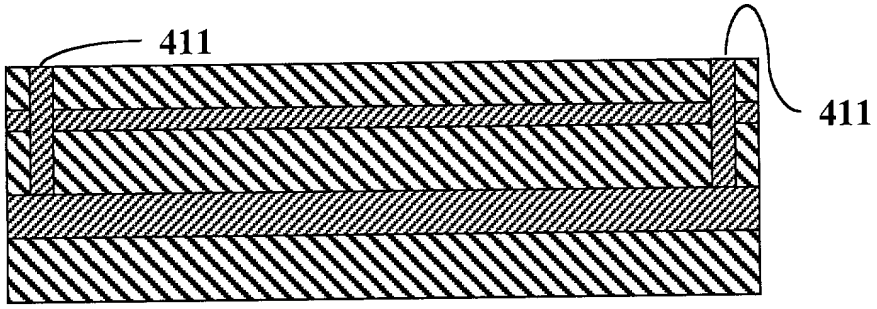


FIG 4C

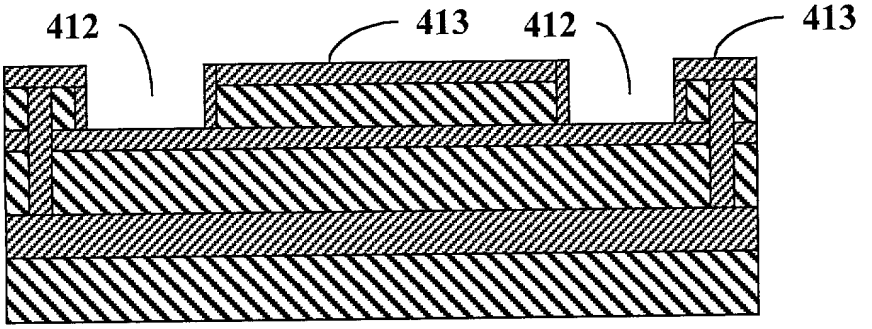


FIG 4D

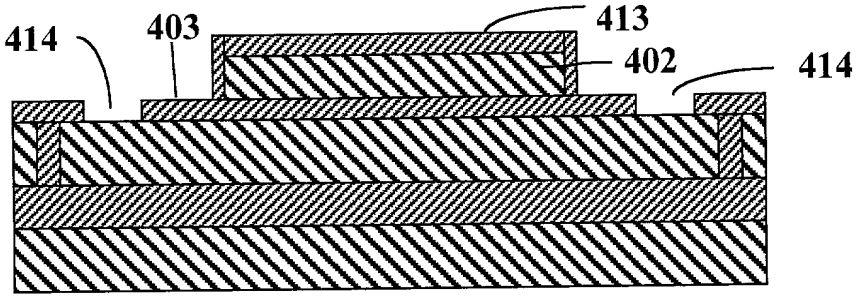


FIG 4E

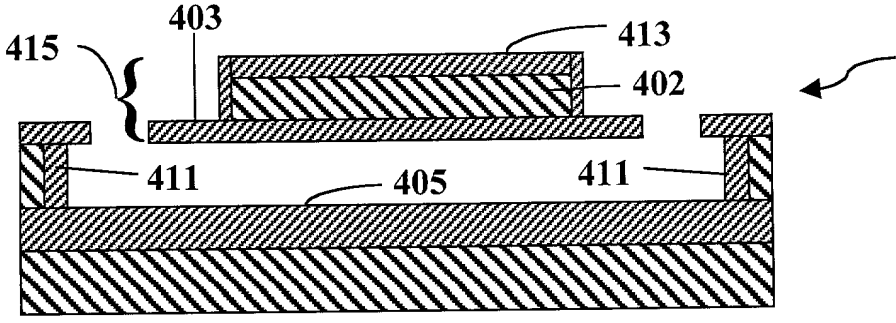


FIG 4F

Declaration for Patent Application and Power of Attorney

As a below named inventor, I hereby declare that my residence, post office address, and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one is listed) or an original, first and joint inventor (if plural names are listed) of the subject matter which is claimed and for which a patent is sought on the invention described in the attached specification entitled

Fabrication and Controlled Release of Structures Using Etch-Stop Trenches.

First or Sole Inventor:	Full name:	**MICHAEL J. DANEMAN**	Citizenship:	**U.S.A.**
	Residence:	**443 Gateway Dr., Pacifica, CA 94044**		
	Postal Address:	**same as above**		
Second Joint Inventor (if any):	Full name:	**BEHRANG BEHIN**	Citizenship:	**U.S.A.**
	Residence:	**2427 Hilgard Ave. #23, Berkeley, CA 94709**		
	Postal Address:	**same as above**		

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)

Country	Application Number	Date of Filing	Priority Claimed Under 35 U.S.C. §119
NONE			[ ] Yes [ ] No

I claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing data of this application.

PRIOR U. S. APPLICATION(S)

Application No.	Filing Date	Status			
60/192,144	**3/24/2000**	[x] Provisional	[ ] Patented	[ ] Pending	[ ] Regular

I hereby appoint Thomas J. McFarlane, Reg. No. 39,299, Marek Alboszta, Reg. No. 39,894, Joshua D. Isenberg, Reg. No. 41,088, Rena Kaminsky, Reg. No. 46,818 as my agents with full power of substitution to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith. Direct all correspondence to:

Joshua D. Isenberg
45 Cabot Ave., Suite 110
Santa Clara, CA 95051
tel: (408) 260-7300
fax: (408) 260-7301

The attorney docket number for this case is: **ONX-109**.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Title 18, §1001 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

INVENTOR SIGNATURE(S)

MICHAEL J. DANEMAN	10/24/00 Date	**BEHRANG BEHIN**	10/24/00 Date

Attorney Docket No: **ONX-109**

POWER OF ATTORNEY BY ASSIGNEE

The undersigned assignee of the entire interest in the attached application for Letters Patent for the invention entitled:

Fabrication and Controlled Release of Structures Using Etch-Stop Trenches

by virtue of Assignment recorded concurrently herewith hereby appoints Thomas J. McFarlane, Reg. No. 39,299, Marek Alboszta, Reg. No. 39,894, Joshua D. Isenberg Reg. No. 41,088, Rena Kaminsky Reg. No. 46,818 as its agents to prosecute the attached application and to transact all business in the Patent and Trademark Office connected therewith, said appointment to be to the exclusion of the inventor(s) and their attorney(s) in accordance with the provisions of Rule 32 of the Patent Office Rules of Practice.

Please direct all communication relative to said application to the following correspondence address:

Joshua D. Isenberg
Lumen
45 Cabot Ave., Suite 110
Santa Clara, CA 95051
tel: (408) 260-7300
fax: (408) 260-7301

I am duly authorized to sign this instrument on behalf of assignee corporation. I hereby declare that, to the best of my knowledge and belief, title is in the assignee herein, and I affirm review of the Assignment document concurrently submitted and believe that the attached application has been assigned to assignee herein and that assignee therefore has the right to make this Power of Attorney and Exclusion of Inventor(s).

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

ASSIGNEE:

Onix Microsystems, Inc.
4138 Lakeside Drive
Richmond, CA 94801

Official Authorized to Act on Behalf of Assignee:

Signature: Jim Head

Name: Jim Head

Title: VP Engr.

11/7/00
Date